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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet 1 of 2

Complete if Known	
Application Number	09/243,825
Filing Date	June 25, 1999
First Named Inventor	Derek Wong
Art Unit	2183
Examiner Name	Eric Coleman
Attorney Docket Number	

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number: Number - Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
E.C.	1	US- 5,630,082	05-13-1997	N. Yao et al	
	2	US- 5,651,125	07-22-1997	D. Witt et al	
	3	US- 5,481,743	01-02-1996	M. Baxter	
	4	US- 5,446,912	08-29-1995	R. Colwell et al	
E.C.	5	US- 5,632,023	05-20-1997	S. White et al	
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FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document: Country Code[3] - Number[4] - Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]

Examiner Signature	Eric Coleman	Date Considered	3/19/04

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] Applicant's unique citation designation number (optional). [2] See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet 2 of 2

Complete if Known	
Application Number	09/243,825
Filing Date	June 25, 1999
First Named Inventor	Derek Wong
Group Art Unit	2183
Examiner Name	Eric Coleman
Attorney Docket Number	

OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
E.C.	6	J. JOHNSON, Expansion Caches for Superscalar Machines, A Doctoral Dissertation in Electrical Engineering Department at Stanford University, March 1996, 183 pages, Stanford, CA, USA. File downloaded from Internet.	
	7	E. ROTENBERG ET AL, "Trace Cache: a Low Latency Approach to High Bandwidth Instruction Fetching", Proceedings of the 29th Annual Symposium on Microarchitecture, December 2-4, 1996, IEEE, New Jersey, USA. File downloaded from Internet.	
	8	E. ROTENBERG ET AL, "Trace Processors", Proceedings of Micro-30, December 1-3, 1997, IEEE, New Jersey, USA. File downloaded from Internet.	
	9	J. CRAWFORD AND J. HUCK, "Next Generation Instruction Set Architecture". Presentation slides from 1997 Microprocessor Forum conference. October 14, 1997, San Jose, CA. File downloaded from intel.com Web site.	
	10	J. CRAWFORD AND J. HUCK, "Motivations and Design Approach for the IA-64 64-bit Instruction Set Architecture." Transcript from 1997 Microprocessor Forum conference. October 14, 1997, San Jose, CA. File downloaded from intel.com Web site.	
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	12	D. GALLAGHER ET AL, "Dynamic Memory Disambiguation Using the Memory Conflict Buffer", Proceedings of ASPLOS-VI conference, October 1994. File downloaded from Internet.	
	13	K. WANG and M. FRANKLIN, "Highly Accurate Data Value Prediction using Hybrid Predictors", Proceedings of Micro 30. December 1-3, 1997, IEEE, New Jersey, USA. File downloaded from Internet.	
	14	D. AUGUST ET AL, "A Framework for Balancing Control Flow and Predication", 1997 paper, Center for Reliable and High Performance Computing, University of Illinois, Urban-Champaign, IL. File downloaded from Internet.	
E.C.	15	S. MAHLKE ET AL, "A Comparison of Full and Partial Predicated Execution Support for ILP Processors", ISCA-22, June 1995. Center for Reliable and High Performance Computing, University of Illinois, Urban-Champaign, IL. File downloaded from Internet.	

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